REMARKS

Claims 12-15, 20-25 and 29-37 are allowed. Claims 1, 2, 4, 6, 7, 9, 11 16 19 and 26 stand rejected. In particular, claims 1, 2, 4, 6, 7, 9, 11, 16 and 26 stand under 35 USC § 102(a) as being unpatentable over U.S. Pat. No. 6,212,566 (hereafter Vanhoof). Claims 3, 5, 8, 10, 17, 18, 27 and 28 are objected to for being dependent on a base rejected claim. Claim 19 stands rejected under 35 USC § 103(a) as being unpatentable over Vanhoof in view of US Pat. No. 6,182,203 (hereafter Simar).

Applicant respectfully submits that Vanhoof does not teach or make obvious the subject matter applicant is claiming. Vanhoof relates to a modem system as well as techniques to design and implement such a modem system. One aspect of the design philosophy is that various components communicate with each other via an interprocess communication (IPC) technique. It appears that the Office Action may be implying that Applicants' claim 1 reads on either or both of (1) the process of designing a digital system in which a designer decides which hardware resources will implement which functions or processes; (2) a technique of mere communication between two processes executing on two processors or two processing units and not a transfer of a process. However, applicants' claim 1 relates to transferring a process to execute on another processing unit.

For example, in claim 1, applicant claims:

> 1. (Original) An apparatus comprising:
> a plurality of processing units;
> a monitor to obtain a plurality of monitor values from said plurality of processing units, wherein said monitor is to transfer a process from a first processing unit of said plurality of processing units to a second processing unit of said plurality of processing units in response to said plurality of monitor values.

The Office Action states that Vanhoof teaches a monitor to obtain a plurality of processing units with reference to Col. 40, ll. 23-49 of Vanhoof. Vanhoof discusses that process assignment can be manual or automatic or controlled by a compiler. However, such static techniques to assign processes to resources differ from including a monitor to obtain a plurality of monitor values from processing units and to transfer processes between processing units in response to the obtained values. Such a dynamic process re-assignment technique is not taught or suggested by Vanhoof.

The Office Action also points to Vanhoof Col. 40, ll. 40-65. Again, this section discusses the static partitioning of the design onto separate hardware blocks. Vanhoof discusses high level language (VHDL, C, etc) descriptions of functions or processes and their ultimate mapping to hardware processor blocks that implement the associated function. This is a design technique to decide what hardware will be implemented to satisfy particular functions, not a technique to dynamically transfer processes amongst hardware resources.

The Office Action further refers to Col. 19, ll. 2-17 and Col. 47, ll. 14-49 in regard to applicants' monitor element in claim 1. Applicant respectfully submits that neither of these sections details what applicant has claimed. For example, the passage at Col. 19, ll. 2-17 appears to discuss two hardware blocks. Applicant respectfully submits that this passage does not teach the transfer of processes between these two blocks in response to monitor values obtained from the two blocks.

Likewise, at Col. 47, ll. 14-49, various processes are detailed. However, these processes are not transferred between processing units.

The Office Action may be arguing that either static assignment by designating hardware blocks to perform certain functions at design time or mere interprocess communication satisfy the elements of claim 1. Applicant respectfully submits that neither of these two techniques meets the limitations of claim 1 as discussed.

Thus, applicant respectfully submits that any rejection based on Vanhoof is traversed. Claims 16 and 26 recite limitations such as re-allocating processes in response to monitor information received from the plurality of processing units (claim 16) and a module to periodically transfer processes between processing units (claim 26). Applicant respectfully submits that these techniques are not taught or suggested by Vanhoof.

Conclusion

Applicant has given at least one reason justifying patentability of all claims, and has not attempted to point out the numerous ways to justify patentability of all the different claims.

As to any remaining combinations formed by dependent claims and not specifically addressed, applicant does not concede that they are obvious or anticipated. Rather, rejections of these claims are overcome since at least the base combination is not anticipated nor obvious in view of the prior art. Consequently, applicant submits that there also can be no motivation shown in the art to form the additionally limited combination claimed in such dependent claims since the prior art does not anticipate or make obvious the base combination.

Amendments which are not specifically discussed with respect to overcoming a particular art objection have not been made in order to overcome the prior art.

Applicants submit that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

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Jeffrey S. Draeger, Reg. No. 41,000

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598